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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/763,795	01/22/2004	Mysore P. Divakar	112518.00003	7938

26707 7590 08/15/2005

QUARLES & BRADY LLP
RENAISSANCE ONE
TWO NORTH CENTRAL AVENUE
PHOENIX, AZ 85004-2391

EXAMINER	
PAREKH, NITIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 08/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/763,795	DIVAKAR ET AL.	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,5-13 and 16-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5-13 and 16-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01-22-04* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 1 and 11 are objected to because of the following:

A. The limitations as recited in claims 1 and 11, include " a pin-fin heat sink mounted to substantially an entire surface area of the semiconductor package" an "a heat sink disposed over substantially an entire surface of the thermally conductive encapsulate" respectively.

However, as described in the specification (see Fig. 2), the heat sink is mounted on substantially an entire top surface area of the semiconductor package.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 2, 7, 9, 11-13, 12, 16 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ho et al. (US Pat. 6369455) in view of Yamashita et al. (US Pat. 2004/0145046).

Regarding claims 1, 2, 7, 9, 11-13, 16 and 18, Ho et al. disclose a semiconductor device in a ball grid array (BGA) configuration (Fig. 8), the device comprising:

- a semiconductor die
- a semiconductor package made with an encapsulant/thermally conductive overmolding compound (TCMC- see 210 in Fig. 7; Col. 6, line 34; Col. 1, lines 60-68) disposed on the semiconductor die, and
- a pin shaped/pin-fin heat dissipating piece/pin-fin heat sink (PFHS) mounted to/on a substantially entire top surface area of the encapsulant/TCMC of the package (see 800/801 in Fig. 8), wherein TCMC physically contacts the die to directly transfer/dissipated the heat generated by the die through the TCMC to the PFHS, and
- the PFHS including a base (not numerically referenced- see the bottom portion of 800 in Fig. 8) with a plurality of pin shaped fins/pin-fins (801 in Fig. 8) extending from the base

(Fig. 8; Col. 6, lines 22-57; Col. 1-4).

Ho et al. fails to teach the TCMC containing an epoxy filler and granules which enhance thermal conductivity (TC) of the overmolding compound to a value greater than 2 watts/meter-K.

Yamashita et al. teach using conventional dice/components including heat generating/power components/IC (see 701 in Fig. 7B) in a power device (sections

0076-0078, 0100 and 0101). Yamashita et al. further teach the power device having a thermally conductive and electrically insulating member/molding compound/TCMC comprising a variety of conventional components including thermosetting/epoxy and resin powder/filler/granules, the TCMC having the TC in a range of 1-10 watts/meter-K encapsulating the power components/IC to provide improved thermal dissipation and reduced stress (701 and 704 in Fig. 7B; see sections 0027-0035, 0077 and 0101).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the TCMC containing an epoxy filler and granules which enhance thermal conductivity (TC) of the overmolding compound to a value greater than 2 watts/meter-K and the die being the power semiconductor device as taught by Yamashita et al. so that the desired electrical/power requirements and functionality can be achieved, the thermal dissipation can be improved and the stress can be reduced in Ho et al's device.

4. Claims 5 and 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ho et al. (US Pat. 6369455) and Yamashita et al. (US Pat. 2004/0145046) as applied to claim 1 above, and further in view of Mostafazadeh et al. (US Pat. 5663593).

Regarding claim 5, Ho et al. and Yamashita et al. teach the entire structure as applied to claim 1 above, except the device further including leadframe supporting the semiconductor die.

Mostafazadeh et al. teach a device having a conventional leadframe supporting a semiconductor die (see 114/112 and 120 in Fig. 7), wherein a plurality of wire bonds are coupled between the semiconductor die and the leadframe (see 130 in Fig. 7; Col. 2 and 3).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the leadframe supporting the semiconductor die and the plurality of wire bonds being coupled between the semiconductor die and the leadframe as taught by Mostafazadeh et al. so that the device processing can be simplified in Yamashita et al. and Ho et al's device.

5. Claims 8 and 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ho et al. (US Pat. 6369455) and Yamashita et al. as applied to claims 1 and 11 above, and further in view of Huang et al. (US Pat. 2002/0180035).

Regarding claims 8 and 17, Ho et al. and Yamashita et al. teach the entire structure as applied to claims 1, 7, 11 and 16 above, except the base including scour lines between the pin-fins.

Huang et al. teach a device having a device/devices having a variety of configurations of heat spreader/heat sink-HS (see Fig. 1-7) where the devices comprise a plurality of devices each having respective HS (see 23/2 in Fig. 1 and 2E-2G).

Furthermore, the devices have dicing/scour lines between the HS structures (see the cut along 232 in Fig. 2G and along the dotted lines in Fig. 2E and 2F) to facilitate the dicing and singulation of the devices and to provide the desired HS surface area for each device (sections 0027-0038).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the base including scour lines between the pin-fins as taught by Huang et al. so that the desired surface area for the HS can be achieved and the device processing/cycle time can be improved in Yamashita et al. and Ho et al's device.

6. Claims 10 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ho et al. (US Pat. 6369455) and Yamashita et al. as applied to claims 1 and 11 above, and further in view of Davies et al. (US Pat. 5901041).

Regarding claims 10 and 19, Ho et al. and Yamashita et al. teach the entire structure as applied to claims 1 and 11 above, except a heat slug being disposed above the semiconductor die without contacting the PFHS.

Davies et al. teach a device having a heat sink (HS) and a heat spreader/slug (see 42 and 18 respectively in Fig. 2 and 3) where a heat spreader slug (see 18 in Fig. 2 and 3) is disposed above the semiconductor die without contacting the HS to provide

efficient heat dissipation and improved reliability of conductive connections (Col. 4, lines 30-68).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the heat slug being disposed above the semiconductor die without contacting the PFHS as taught by Huang et al. so that the heat dissipation and reliability can be improved in Yamashita et al. and Ho et al's device.

Response to Arguments

7. Applicant's arguments filed on 06-07-05 have been fully considered but they are not persuasive.

A. Applicant argues that Ho et al. do not rely on using a high TC encapsulate material since the TC of the encapsulate is less than that of the HS.

However, Ho et al. teaches improving the thermal transfer and heat dissipation efficiency through the encapsulate and the heat sink (HS). Using the encapsulate/molding compound having the desired TC as taught by Yamashita et al. provides further enhancement in the heat dissipation efficiency in Ho et al's package. Therefore, Yamashita et al's combination with Ho et al. is proper.

B. Applicant argues that The Yamashita et al's reference do not teach the die directly and physically contacting and encapsulating compound.

However, as shown in Fig. 7B, the IC component is in direct physical contact with the encapsulating compound (see 701 and 704 respectively in Fig. 7B).

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's acting supervisor, Steven Loke can be reached on 571-272-1657. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAN or Public PAG. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAG system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Nitin Parekh

NP

08-08-05

NITIN PAREKH

PRIMARY EXAMINER

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